Amendments to the Claims

Please amend the claims as follows:

1. (currently amended): A method for forming an isolation region comprising the steps of:

providing a region of semiconductor material;

forming a tub in the region of semiconductor material, wherein the tub includes a plurality of shapes in a matrix, wherein adjacent rows of shapes are offset from each other; and

exposing the plurality of shapes to an ambient that includes a chemical species that reacts with the plurality shapes to form the isolation region, and wherein the plurality of shapes form part of the isolation region.

2. (previously presented): The method of claim 1 wherein the step of exposing includes thermally oxidizing the plurality of shapes to form a silicon oxide isolation region.

3. (previously presented): The method of claim 1 wherein the step of forming the tub includes forming the tub having a boundary around the plurality of shapes, wherein the boundary includes a recessed portion.

4. (original): The method of claim 1 wherein the step of exposing includes consuming substantially all of the plurality of shapes.

5. (previously presented): The method of claim 1 further comprising the step of forming a passive device over the isolation region.

6. (previously presented): The method of claim 1 wherein the step of forming the tub includes etching exposed portions of the region of semiconductor material, and wherein the plurality of shapes comprise unexposed portions of the region of

semiconductor material.

7. (original): The method of claim 6 wherein the step of etching includes etching to a depth from about 6 microns to about 10 microns.

8. (canceled): The method of claim 1, wherein the step of forming the tub includes forming a tub having a matrix of free standing shapes, wherein adjacent rows of shapes are offset from each other.

9. (original): The method of claim 1 wherein the step of providing the region of semiconductor material includes providing a region comprising silicon.

10. (previously presented): A process for forming an integrated circuit device including the steps of:

forming a tub region within a semiconductor layer, wherein tub region includes a matrix of shapes comprising offset rows; and

forming a dielectric region within the matrix of shapes.

11. (previously presented): The process of claim 10 wherein the step of forming the tub region includes forming a tub region with a matrix of squares.

12. (original): The process of claim 10 wherein the step of forming the dielectric region includes oxidizing the matrix of shapes.

13. (original): The process of claim 12 wherein the step of oxidizing forms a nearly continuous silicon oxide tub.

14. (original): The process of claim 10 further comprising the step of forming a passive component over the dielectric region.

15. (original): The process of claim 10 further comprising the step of forming an isolation trench in the region of semiconductor material.

16. (original): The process of claim 10 further comprising the steps of:

forming a dielectric layer on sidewalls of the matrix of shapes; and

forming a polycrystalline semiconductor layer over the dielectric layer.

17. (previously presented): The process of claim 10 wherein the step of forming tub region includes forming tub region having a matrix of shapes wherein shapes in a first row have a first spacing, and wherein the shapes in the first row have a second spacing from shapes in a second row, and wherein the second spacing is less than the first spacing.

18. (previously presented): A semiconductor device comprising:

a region of semiconductor material; and

a dielectric tub formed in the region of semiconductor material, wherein the dielectric tub includes a matrix of passivated shapes, and wherein adjacent rows of passivated shapes are offset.

19. (original): The device of claim 18 wherein the dielectric tub comprises oxidized silicon shapes.

20. (original): The device of claim 18 wherein the dielectric tub includes a boundary having a recessed portion.